

正本

# 經濟部智慧財產局 函

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速別：速件  
密等及解密條件：  
發文日期：中華民國九十一年十一月四日  
發文字號：(九一)智專二(六)0188字第0九一二〇二四一二號  
附件：

主旨：請於文到次日起六十日內，提出第〇九〇一一〇二三四號專利申請案補充說明、申請專利範圍修正本一式三份、及修正規費壹仟元，送局憑辦，逾限或不同意補充、修正，本局即依原申請內容逕予審定，請查照。

說明：

一、依專利法第四十四條之一規定辦理。

二、本案經審查認為：

(一) 本案「製備具低介電常數之絕緣材料的方法」申請專利範圍主項過廣，和已公開之技術資料，有重複之嫌，如EP 0997497、US 5955786、JP 200002187。申請人應提出說明本案與引證案之差異或具不可推知之進步性。

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雙掛

發文文號：09111021412

第二頁

- (二) 本案申請專利範圍第一項過廣，應予刪除，而改以第二項為主體，但第二項之各記號之範圍過廣遠超出實例可支持範圍，應限制在有實例可資證明範圍內方可，其附屬項也同。
- (三) 本案申請專利範圍第十一項無實例測試其分子量，無具體資料證明，應將第十一項刪除之。
- (四) 本集中譯不妥之處，如一頁第5行、第二頁、實例6（應該是實例7），應修正。

正本：L G 化學投資股份有限公司（代理人：惲軼群先生、陳文郎先生）

副本：

局長 蔡練生

依照分局負責規定  
授權單位主管決定

c:\A9100351.329

第三頁

\*09111021412\*

(ENGLISH TRANSLATION)

**OFFICIAL LETTER**

Date of Receipt: November 6, 2002

From : THE INTELLECTUAL PROPERTY BUREAU  
MINISTRY OF ECONOMIC AFFAIRS

To : LG CHEM INVESTMENT, LTD.  
C/o : PATRICK I.C. YUN AND WILLIAM W.L. CHEN, patent attorneys

**SUBJECT**

An amendment of the claims of Patent Application No. 90110234 should be submitted, in triplicate, within sixty (60) days of the day following the date of receipt of this Official Letter. **This deadline cannot be extended.** Failure to comply with the requirement, or a late reply, will result in the rejection of this application.

**CONTENTS**

1. The claimed scope of the present invention, entitled "A process for preparing insulating material having low dielectric constant," is too broad and might cover published technical references, such as EP 0997497, US 5955786 and JP 200002187. The Applicant should clarify the differences between this invention and these cited references or the nonobviousness of this invention therefrom.
2. Claim 1 in this application is too broad and should be deleted and Claim 2 should be made the main claim. However, the scope of each substituent in Claim 2 is too broad and exceeds the scope that can be supported by the examples, and thus, should be limited to that which can be corroborated by the examples, and so should the dependent claims thereof.
3. Claim 11 in this application is not corroborated by any example of measuring the molecular weight thereof, and, being devoid of such confirmatory data, should be deleted.

Sealed by

The Intellectual Property Bureau  
Ministry of Economic Affairs

Search Strategy  
(Word)(insulating material) and (Word)(low dielectric constant)

131:222082

Semiconductor device fabrication using uniform nonconformal deposition for forming low dielectric constant insulator between certain conductive lines.

Avanzino, Steven; Erb, Darrell; Cheung, Robin; Klein, Rich (Advanced Micro Devices, Inc., USA). U.S. US 5955786 A 21 Sep 1999, 10 pp. (English). (United States of America).

CODEN: USXXAM. CLASS: ICM: H01L023-48. ICS: H01L023-52; H01L029-40. NCL: 257758000. APPLICATION: US 1995-481906 7 Jun 1995. DOCUMENT TYPE: Patent CA

Section: 76 (Electric Phenomena)

A method of forming low dielec. insulation between those pairs of conductive lines, of a level of interconnection for integrated circuits, having a gap of  $\sim 0.5 \mu\text{m}$  or less by depositing a nonconformal source with a poor step function for the **insulating material**, such as silane as the Si source for  $\text{SiO}_2$ , so as to create, in the gap, a large void whose dielec. const. is slightly  $>1$ .

After the formation of the void in the  $0.5 \mu\text{m}$  or less gaps, the deposition of the nonconformal source material is stopped and a flowable **insulating material**, such as spin on glass, is coated on nonconformal **insulating material** to fill the remaining gaps. After etching the surfaces of the nonconformal and flowable insulating materials, another insulating layer is deposited and planarized to the desired overall thickness of the insulation. Alternatively, a thin conformal insulating layer is 1st deposited as a liner on the conductive lines. The resulting structure of the interconnection level comprises a layer of insulation between and on the conductive lines with the dielec. const. of the insulation between the pairs of conductive lines with gap of  $0.5$  or less being, in combination with the void, at least  $\sim 3$  or lower, and substantially all of the remaining gaps are filled with the flowable **insulating material** and are void free with a composite dielec. const. of  $\sim 3.5$ .

